SELF-HEALING CELLULAR AUTOMATA (SHCA) FOR DEFECTIVE EMBEDDED-PROGRAM MEMORIES
Reliability of nano-scale SRAM

Random Dopant Fluctuations [1]

Sub-threshold Operation [2]

Threshold Variations [3]

Large scale massively distributed Soft Errors

0.2 V, a 0.025V variation in threshold voltage, thermal noise => mean time for a bit flip error (10^-8 seconds) [3]

Current Research – Quantity, frequency and orientation of Soft Errors

1. Do we need anything more than single bit error correction (ECC)? [4]
2. Can an error correction technique correct errors in a target circuit/system if it’s contents/circuit itself malfunction?

[4] Spica, M.; Mak, T.M., "Do we need anything more than single bit error correction (ECC)?"
Inherent Redundancy Analysis

- Error correction techniques largely depend on redundancy

- Are there systems that have Inherent Redundancy (an artifact of possibly some other optimization process)?

- Experiments (Chip Multiprocessors)
  - A case of 3 programs (three instance of matrix multiplication, FIR implementation, Integer Transform)
  - A case of 9 programs (one instance of bubble sort, selection sort, quick sort, shell sort, DWT lifting kernel, heap sort, h.264 4x4 integer transform, quick sort and cocktail sort)
### Contours in Program Mixtures

Contour is a set of similar instructions spread across all program memories considered. The goal is to make all instructions participate in the contour map.
Results for Inherent Redundancy Analysis

**Case 1** (matrix multiplication, FIR implementation, Integer Transform)
Average increase in code length – 71%

**Case 2** (bubble sort, selection sort, quick sort, shell sort, DWT lifting kernel, heap sort, quick sort, h.264 4x4 integer transform, and cocktail sort)
Average increase in code length – 500%

**Code Increase for case 1**

Inter-processor compiler approach
- Programs having same RISC ISA considered
- Results differ based on size, program types
- No conclusions drawn on quality of approach
Majority Rule and Reconfigurable RT

Boolean Expression = \( c \cdot e + c \cdot n + \overline{c} \cdot s \cdot w \)

Reconfigurable Rule Table
Bit Planes & CIB

Bits in Red - Errors

SHCA
Self Healing Process

Dedicated (3x3) SHCA for CIB

9 Contour Information Banks

(NxN) x log2(m)

NxN Program Memories

b (NxN) SHCA Networks

Micron Research Center
Number of iterations vs Percentage corruption for Corrupted and perfect SHCA.

Comparison of SHCA performance with and without Self-Healing.
Comparison with other ECC Techniques

Comparison with Hierarchical Ternary TMR Voter and SEC-DED Hamming for 16 bits per instruction

Comparison with Reed Solomon* for 144 Embedded Program Memories, with 160 instructions per Memory and 12 bits per instruction**.

*Implemented using Xilinx IP cores.
**All the CIB’s are mapped on to 4-input LUTs and not BRAMs on an FPGA (Xilinx Virtex4 LX60).
Future Work

• A compile time optimization algorithm to effectively identify possible inherent redundancy with a constraint on minimal code length increase

• Efficient method to store the contour information bank

• A smart way to perform self repair of the SHCA